**What is claimed is:**

1. A method of manufacturing chalcogenide memory in a semiconductor substrate comprising the steps of:

forming a N+ epitaxy layer on the semiconductor substrate;

forming a N- epitaxy layer on the N+ epitaxy layer;

forming a first shallow trench isolation (STI) in the N+ and N- epitaxy layers to isolate a predetermined word line region;

forming a second STI in the N- epitaxy layer to isolate a predetermined P+ doped region;

forming a dielectric layer on the N- epitaxy layer;

patterning the dielectric layer to form a first opening and performing a N+ doping on the N- epitaxy layer via the first opening such that a N+ doped region is formed in the N- epitaxy layer and connected to the N+ epitaxy layer;

patterning the dielectric layer to form a second opening and performing a P+ doping in the N- epitaxy layer such that a P+ doped region is formed;

forming contact plugs in the first opening and the second opening respectively; and

forming an electrode on each contact plug, wherein the electrode includes a lower electrode, a chalcogenide layer and an upper electrode.

2. The method as recited in claim 1, wherein the N+ epitaxy layer has a thickness of 400 to 600 angstroms.

3. The method as recited in claim 1, wherein the N- epitaxy layer has a thickness of 800 to 1200 angstroms.

4. The method as recited in claim 1, wherein the first STI is formed in the N+ epitaxy layer and the N- epitaxy layer.

5. The method as recited in claim 1, wherein the first STI is formed by a dry or wet etching.

6. The method as recited in claim 1, wherein the second STI is formed by a dry or wet etching.

7. The method as recited in claim 1, wherein the N+ doping is accomplished by implanting arsenic or phosphorus.

8. The method as recited in claim 7, wherein the N+ doping comprises a dosage between $10^{15}$ and 2 x $10^{16}$ atoms/$cm^2$ and energy between 10 and 30 keV.

9. The method as recited in claim 1, wherein the P+ doping is accomplished by implanting boron.

10. The method as recited in claim 9, wherein the P+ doping further comprising a dosage between $10^{15}$ and 1 x $10^{16}$ atoms/$cm^2$ and energy between 1 and 3 keV.

11. The method as recited in claim 1, wherein the dielectric layer comprises tetra-ethyl-ortho-silicate.

12. The method as recited in claim 1, wherein the dielectric layer has a thickness of 2000 to 3000 angstroms.

13. A structure of chalcogenide memory, comprising:
a semiconductor substrate;
a N+ epitaxy layer formed on the semiconductor substrate;
a N- epitaxy layer formed on the N+ epitaxy layer;
a first STI formed in the N+ and N- epitaxy layers to isolate a word line region;

a P+ doping region formed in the N- epitaxy layer;

a second STI formed in the N- epitaxy layer to isolate the P+ doped region;

a N+ doped region formed in the N- epitaxy layer and connected to the N+ epitaxy layer;

contact plugs formed on the N+ doped region and the P+ doped region respectively; and

an electrode formed on each contact plug, wherein the electrode includes a lower electrode, a chalcogenide layer and an upper electrode.

14. The structure as recited in claim 13, wherein the N+ epitaxy layer has a thickness of 400 to 600 angstroms.

15. The structure as recited in claim 13, wherein the N- epitaxy layer has a thickness of 800 to 1200 angstroms.

16. The structure as recited in claim 13, wherein the first STI is formed in the N+ epitaxy layer and the N- epitaxy layer.

17. The structure as recited in claim 13, wherein the first STI is formed by a dry or wet etching.

18. The structure as recited in claim 13, wherein the second STI is formed by a dry or wet etching.

19. The structure as recited in claim 13, wherein the N+ epitaxy layer is formed by selective epitaxial method.

20. The structure as recited in claim 13, wherein the N- epitaxy layer is formed by selective epitaxial method.